**High-Level Model of c2670**

**Statistics:** 233 inputs; 140 outputs; 1193 gates

**Function:** 12-bit ALU and controller

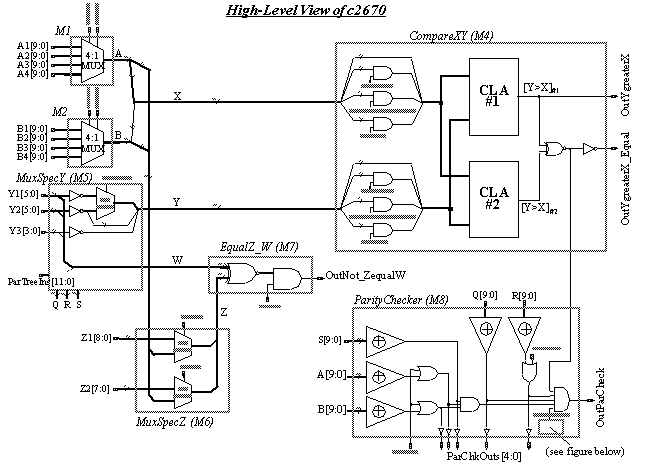
This benchmark consists of an ALU with a comparator, an equality checker, and several parity trees. The comparator has two 12-bit inputs X and Y, and computes Y>X using a carry-lookahead adder (CLA) that performs the addition !X+Y. It can be programmed to do a 4, 6, 8 or 12-bit comparison of its inputs. An interesting feature of the comparator is that it uses two identical CLAs that have identical inputs, a redundancy technique commonly used in fault-tolerant systems. The CLAs have a fairly standard structure with 3, 4 and 5-bit blocks. The carry output signal of each CLA gives the result of (Y>X). The output labeled *OutYgreaterX\_Equal* (line number 231) is constant 1 if the outputs of the two CLAs are identical, as would normally be the case. If, however, the CLAs produced different results, the *OutYgreaterX\_Equal* output would be **logic 0**, implying an error in the circuit. This would happen, for example, if there were manufacturing defects in one of the CLAs.

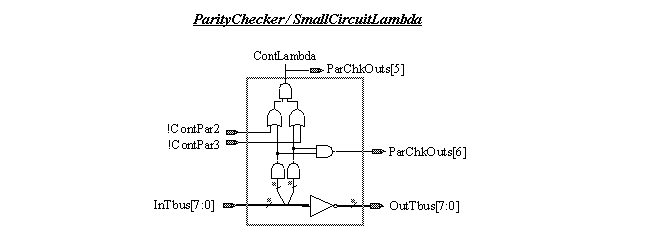
Module M7 *(EqualZ\_W)* performs an equality check on two 17-bit buses. The *ParityChecker* module (M8) contains five 10-input parity trees, whose outputs are all ANDed. This module seems to perform a sanity check on the input buses of c2670. There are also several small pieces of logic which are mostly random.

[**Inputs/Outputs vs. Netlist Numbers**](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c2670/c2670.html#pgfId=1006502)

**Models:**

* I. Original ISCAS gate-level netlist
  + [in ISCAS-89 format](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c2670/c2670.isc)
  + [in Verilog](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c2670/c2670gate.v)
* II. [Verilog hierarchical netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c2670/c2670high.v) (functionally equivalent to I)
* III. [Verilog flat netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c2670/flat2670.v) (flat version of II; functionally equivalent to I, but with minor structural differences)





**\* Netlist numbers for input buses A[9:0] and B[9:0]:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input bus | | 0[lo] | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 [h] |
| A | A1 | 81 | 92 | 91 | 90 | 89 | 88 | 87 | 86 | 85 | 93 |
| A2 | 43 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 55 |
| A3 | 56 | 66 | 65 | 64 | 63 | 62 | logc1 | 61 | 60 | 67 |
| A4 | 68 | 79 | 78 | 77 | 76 | 75 | 74 | 73 | 72 | 80 |
| B | B1 | 131 | 141 | 140 | 139 | 138 | 137 | 136 | 135 | 142 | **logic1** |
| B2 | 95 | 105 | 104 | 103 | 102 | 101 | 100 | 99 | 106 | **logic1** |
| B3 | 119 | 129 | 128 | 127 | 126 | 125 | 124 | 123 | 130 | **logic1** |
| B4 | 107 | 117 | 116 | 115 | 114 | 113 | 112 | 111 | 118 | **logic1** |

**\* Input buses Y1[5:0], Y2[5:0], Y3[3:0]:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | 0 [lo] | 1 | 2 | 3 | 4 | 5 [h] |
| Y1 | 1341 | 1348 | 1956 | 1961 | 1966 | 1971 |
| Y2 | 1996 | 2067 | 2072 | 2078 | 2084 | 2090 |
| Y3 | 1976 | 1981 | 1986 | 1991 | - | - |

**\* Inputs X[11:0] and Y[11:0] of CompareXY (M4):**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 0[lo] | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11[h] |
| X | A[0] | A[1] | A[2] | A[3] | A[4] | A[5] | A[6] | A[7] | A[8] | B[0] | B[1] | B[2] |
| Y | Y1[0] | Y1[1] | Y1[2] | Y1[3] | Y1[4] | Y1[5] | Y3[0] | Y3[1] | Y3[2] | Y3[3] | Y2[0] | Y2[1] |
| Y2[0] | Y2[1] | Y2[2] | Y2[3] | Y2[4] | Y2[5] |

**\* Inputs W[16:0] and Z[16:0] of Bitwise Comparator (M7):**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 0[lo] | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16[hi] |
| Z | A[0] | A[1] | A[2] | A[3] | A[4] | A[5] | A[6] | A[7] | A[8] | B[0] | B[1] | B[2] | B[3] | B[4] | B[5] | B[6] | B[7] |
| 19 | 4 | 20 | 5 | 21 | 22 | 23 | 6 | 24 | 25 | 32 | 26 | 33 | 27 | 34 | 35 | 28 |
| W | Y1[0] | Y1[1] | Y1[2] | Y1[3] | Y1[4] | Y1[5] | Y3[0] | Y3[1] | Y3[2] | Y3[3] | Y2[0] | Y2[1] | Y2[2] | Y2[3] | Y2[4] | Y2[5] | **logic0** |

**\* Q[9:0], R[9:0], S[9:0] (inputs to ParityChecker M8) are three 10-bit buses multiplexed out of Y1, Y2, Y3 and ParTreeIns:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 0 [lo] | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 [hi] |
| Q | Y1[2] | Y1[3] | Y1[4] | Y1[5] | Y3[0] | Y3[1] | Y3[2] | Y3[3] | Y2[0] | 2474 |
| R | Y1[0] | Y1[1] | 2427 | 2430 | 2451 | 2454 | 2443 | 2446 | 2435 | 2438 |
| S | Y2[2] | Y2[3] | Y2[4] | Y2[5] | Y2[1] | 2096 | 2100 | 2678 | **logic0** | **logic0** |

**\* Netlist numbers for the remaining inputs:**

|  |  |
| --- | --- |
| Inputs | Netlist numbers |
| ContA0, ContA1 | 651, 543 |
| ContB0, ContB1 | 2105, 2104 |
| ContZ0. ContZ1 | 16, 29 |
| ContEq | 11 |
| ContMask0,1,2 | 8, 1384, 40 |
| ContAlpha | !B[5]. ContMask2. B[4]. !ContMask1 |
| ContBeta | !B[5]. ContMask2. (!B[4] + ContMask1) |
| ContPar0,1,2,3 | 14, 37, 2106, 567 |
| ParTreeIns[11:0]  (fanin of Q,R,S) | 2096, 2100, 2678, 2454, 2451, 2446, 2443, 2438, 2435, 2430, 2427, 2474 |
| InTbus[7:0] | 108, 57, 120, 69, 96, 82, 132, 44 |
| MiscRandomIns[11:0] | 3, 1, 483, 36, 15, 2, 661, 7, 94, 1083, 2066, 452 |
| MiscMuxIn | 559 |
| MiscMuxCont0,1 | 868, 860 |

**\* Netlist numbers for outputs:**

|  |  |
| --- | --- |
| Outputs | Netlist numbers |
| OutYgreaterX (Y>X) | 329 |
| OutYgreaterX\_Equal  (Y>X)#1 == (Y>X)#2 | 231 |
| OutZequalW (Z==W) | 150 |
| OutNot\_ZequalW (Z != W) | 311 |
| OutParCheck | 308 |
| OutNot\_ParCheck | 225 |
| ParChkOuts[7:0] | 261, 325, 319, 401, 229, 227, 397, 395 |
| OutTbus[7:0] | 238, 237, 236, 235, 221, 220, 219, 218 |
| MiscMuxOuts[10:0] | 280, 321, 323, 331, 153, 148, 145, 297, 284, 282, 295 |
| MiscBusOuts[12:0] | 164, 160, 162, 171, 168, 166, 299, 301, 286, 303, 288, 305, 290 |
| MiscRandomOuts[17:0] | 158, 188, 176, 259, 234, 217, 223, 156, 173, 369, 367, 411, 384, 337, 409, 391, 350, 335 |